Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.   (Currently Amended) An authorization control circuit in an electronic device, comprising:
a digital signal processor operable to provide digital data output, determine an authorization state, and generate a disable signal;
a digital to analog converter coupled to the digital signal processor and operable to receive the digital data output, convert the digital data to corresponding analog data, output the corresponding analog data, and mute the output of the corresponding analog data; and
the converter including an input operable to receive the disable signal, and the converter muting the output of the corresponding analog data in response to the disable signal, wherein the disable signal is generated when the electronic device satisfies one or more sleep conditions.

2.   (Original) The circuit of Claim 1, wherein the authorization state is either positive or negative and the digital signal processor is operable to generate the disable signal when the authorization state is negative.

3.   (Original) The circuit of Claim 1, the converter further comprising a serial input for receiving timing signals to enable reception of the disable signal.

4.   (Original) The circuit of Claim 1, wherein the analog output is muted by filtering the received digital data prior to conversion into analog data.

5.   (Original) The circuit of Claim 1, the digital signal processor further comprising:
an output pin operable to transmit the disable signal as a high voltage.

6.   (Original) The circuit of Claim 1, the converter further comprising:
a pull-down circuit operable to create a low voltage at the input in the absence of a disable signal.

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7.   (Original)   The circuit of Claim 1, wherein the authorization state is either positive or negative and the digital signal processor is not operable to generate the disable signal when the authorization state is negative.

8.   (Original) The circuit of Claim 1, wherein the digital signal processor has at least two output pins, the first pin provides a clock signal, the second pin provides the disable signal, and the state of the disable signal at the rising edges of the clock signal are read by the converter.

9.   (Currently Amended)   An authorization control circuit in an electronic device, comprising:

a digital signal processor operable to provide digital data output, determine an authorization state, and generate a disable signal;

a digital to analog converter coupled to the digital signal processor and operable to receive the digital data output, convert the digital data to corresponding analog data, and output the corresponding analog data; and

an analog amplifier operable to receive the analog output from the converter and generate amplified output, and having an input operable to receive the disable signal, the amplifier muting the amplified output in response to the disable signal, wherein the disable signal is generated when the electronic device satisfies one or more sleep conditions.

10.   (Original)   The circuit of Claim 9, wherein the authorization state is either positive or negative and the digital signal processor is operable to generate the disable signal when the authorization state is negative.

11.   (Original)   The circuit of Claim 9, wherein the authorization state is either positive or negative and the digital signal processor is not operable to generate the disable signal when the authorization state is negative.

12.   (Currently Amended)   A method of selectively muting output, comprising the steps of:

generating digital data;

determining an authorization state, wherein determining the authorization state comprises comparing a mathematical function result to an expected result;

generating a disable signal;

transmitting the digital data to a digital to analog converter;

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generating an analog signal corresponding to the digital data;

transmitting the disable signal to the digital to analog converter; and

muting the analog signal in response to the transmitted disable signal.

13.   (Original)   The method of Claim 12, wherein the step of muting comprises activating a digital filter.

14.   (Original) The method of Claim 12, wherein the step of muting comprises signal processing that occurs after the step of generating the analog signal.

15.   (Original)   The method of Claim 12, wherein the authorization state is either positive or negative and the disable signal is generated after the authorization state is determined to be negative.

16.   (Original) The method of Claim 12, further comprising the step of:

generating a clock signal and wherein the step of muting is in response to the state of the disable signal at the rising edges of the clock signal.

17.   (Original)   The method of Claim 16, wherein the clock signal is transmitted contemporaneously with the disable signal.

18.   (Original) The method of Claim 12, further comprising the step of:

generating a power-save signal and wherein the disable signal is generated in response to the power-save signal.

19.   (Currently Amended)   The method of ~~claim~~ Claim 12, further comprising the steps of:

generating an override signal; and

terminating the muting step in response to the override signal.

20.   (Currently Amended) The method of ~~claim~~ Claim 19, further comprising the step of:

detecting the step of generating the disable signal; and wherein the override signal is generated in response to the detection of the disable signal.

21.   (New) The circuit of Claim 1, wherein one of the sleep conditions is usage of the electronic device, said disable signal generated when the usage meets a predetermined criteria.

22.   (New) The circuit of Claim 1, wherein the electronic device is a music player, video player, or multimedia file player.

23.   (New) The method of Claim 12, wherein the step of determining an authorization state further comprises:

selecting a data file, wherein the data file includes the digital data; and

performing a hashing function on the data file to generate the mathematical function result, wherein the hashing function is executed by a digital signal processor.